GOC-N78690P V1.1

Bluetooth+WIFI Module Hardware Specification

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NOTES:

1. **The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.**
2. **Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.**

Release Record

Version Number	Release Date	Comments
V1.0	2020/10/20	Initial draft

Contents

1. Introduction

The GOC-N78690P is a highly integrated, IEEE 802.11ax Concurrent Dual Wi-Fi (CDW) and Bluetooth combo solution that supports simultaneous 2.4 GHz and 5 GHz WLAN operation targeted for automotive In-Vehicle Infotainment (IVI) applications.

The GOC-N78690P is a next generation, High Efficiency Wireless (HEW) product and is backward compatible with 802.11ac Wave1 and Wave2 technology.

Host interfaces include PCI Express for connecting WLAN and Bluetooth technologies to the host processor. A High-Speed UART interface is also included for connecting Bluetooth to the host processor.

2. Block Diagram

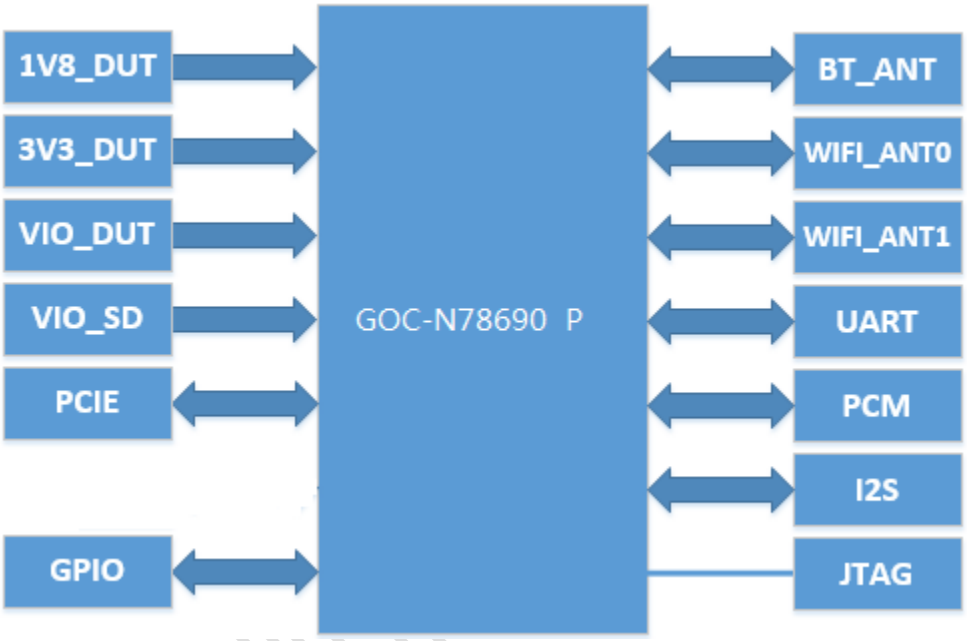

Figure 1: GOC-N78690P System Block Diagram

3. Features

- 2x2 5 GHz 802.11ax + 2x2 2.4 GHz 802.11n
- 2x2 5 GHz 802.11ac (40 MHz) + 2x2 2.4 GHz
- 802.11ax
- 5 GHz PHY data rates up to 1.2 Gbps
- 2.4 GHz PHY data rates up to 458 Mbps
- MU-MIMO and OFDMA
- 2x Wide Band Speech (WBS) channel for simultaneous Hands-Free Profile (HFP) support on smartphones
- Firmware SDK to develop differentiated features and applications
- AEC-Q100 Grade 3 (85℃extended temperature)

3.1 WLAN

- 802.11ax 2x2 SU and MU-MIMO/OFDMA
- 802.11ac Wave 1/Wave 2 backward compatible
- 802.11n/a/g/b backward compatible
- 802.11e quality of service
- 802.11h transmit power control

- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11mc precise indoor location positioning
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception
- 802.11w protected management frames
- 802.11z tunneled direct link setup
- Fully supports clients (stations) implementing IEEE
- Uplink MU-MIMO Tx
- Downlink MU-MIMO Rx
- Uplink OFDMA Tx
- Downlink OFDMA Rx
- Downlink VHT MU-MIMO Rx
- Tx support up to 2 streams as UL-MU Tx client
- Rx support up to 2 streams as DL-MU Rx client
- Various MCS/Spatial Stream/Coding combinations
- Arbitrary Resource Unit (RU) sizes and allocations for UL-OFDMA Tx and DL-OFDMA Rx
- Up to 2 spatial streams per RU
- Various MCS/Spatial Stream/Coding combinations
- 2.4 GHz or 5 GHz bands

3.1.1 WLAN Dual-MACs

- Dual, independent MACs (with dual-Baseband and dual-WLAN radios) support true, simultaneous
- WLAN network operation at 2 different frequency bands
- Trigger Frame Formats
  - Basic trigger frame
  - Beamforming Report Poll (BRP)
  - MU-BAR, MU-RTS, BSR Poll (BSRP) trigger variant
  - Trigger frame MAC padding
- HE Variants of HT Control
  - Basic format
  - UL Power Headroom
  - Receive Operation Mode control subfield
- HE MU Frame Exchange Sequences
- MU Acknowledgment (ACK)
- M-BA and C-BA Variants in BA Frames
- MU-RTS/CTS Procedures
- TWT Scheduling
- HE Dual-NAV
- UL Carrier Sensing
- Buffer Status Reports
- Operating Mode Indication (OMI)
- Multiple-BSS/Station
- A-MPDU Rx (de-aggregation) and Tx (aggregation)(supports single-MPDU A-MPDU)
- Management information base counters
- Transmit rate adaptation
- Transmit power control

- Marvell mobile hotspot
- Dynamic Congestion Control (DCC)

3.1.2 WLAN Encryption

- Data Frame Encryption/Decryption
  - WEP
  - TKIP
  - AES/CCMP
  - AES/GCMP
  - WAPI
- Management Frame Encryption/Decryption for broadcast/multicast packets
  - AES/CMAC
- Management Frame Encryption/Decryption for unicast packets
  - AES/CCMP
  - AES/GCMP

3.1.3 Transmit Beamforming (TxBF)

- Marvell Implicit Beamforming
  - Supports all devices
  - Beamforming up to 2 streams
- 802.11ax/ac/n Explicit Beamformer
  - NDP sounding to stations capable of explicit beamformee
  - Beamforming up to 2 streams
- 802.11ax/ac/n Explicit Beamformee
  - Supports high-resolution compressed SU/MU immediate feedback
  - 8 Nsts capability for up to 80+80 (802.11ax/ac only)

3.1.4 WLAN Dual-Basebands

- Dual, independent Basebands (with dual-MAC and dual-WLAN radios) support true,simultaneous
- WLAN network operation at 2 different frequency bands Backward compatibility with legacy 802.11ac/n/a/g/b technology
- 5 GHz PHY data rates up to 1.2 Gbps
- 2.4 GHz PHY data rates up to 458 Mbps
- Bandwidth support
  - 20 MHz
  - 40 MHz
  - 80 MHz
  - 80+80 MHz
- Modulation and Coding Schemes (MCS)
  - 802.11ax—MCS 0~11
  - Up to 2 spatial streams for 20, 40, 80 MHz
  - Up to 1 spatial stream for 80+80 MHz
  - 802.11ac—MCS 0~9 Nsts = 1 and 2
  - Up to 2 spatial streams for 20, 40, 80 MHz
  - Up to 1 spatial stream for 80+80 MHz
  - 802.11n—MCS 0~15 and MCS 32 (duplicate 6 Mbps)

- Dual Sub-Carrier Modulation (DCM)
- MCS 0 only
- BCC and LDPC coding
- 1 spatial stream STBC across all frame formats

- Frame Formats
  - 802.11ax HE_SU (Tx/Rx)
  - 802.11ax HE_MU (Rx)
  - 802.11ax HE_ER_SU (Tx/Rx)
  - 802.11ax HE_TB (Tx)
  - 802.11ac VHT
  - 802.11n HT
  - 802.11a (including dup/quad/oct modes)
  - 802.11g (including dup mode)
  - 802.11b
- Packet Extension
  - Up to 8 µs for highest rates
  - 0 µs for all other modes
- Range Extension
- Beam Change
- Guard Interval Modes
  - 1x HE-LTF with 0.8 µs GI
  - 1x HE-LTF with 1.6 µs GI (for UL TB PPDU)
  - 2x HE-LTF with 0.8 µs GI
  - 2x HE-LTF with 1.6 µs GI
  - 4x HE-LTF with 3.2 µs GI
  - 4x HE-LTF with 0.8 µs GI
- Dynamic frequency selection (radar detection)
- Optional 802.11ac and 802.11n MIMO features:
  - 20/40/80/80+80 MHz coexistence with middle-packet detection (GI detection) for enhanced CCA
  - 1 spatial stream STBC reception and transmission
  - LDPC transmission and reception for both 802.11ac and 802.11n
  - 256 QAM (MCS 8, 9) modulation (optional support for 802.11ac MCS 9 in 20 MHz using LDPC)
  - Short guard interval (0.4 µs)
  - RIFS on receive path for 802.11n packets
  - VHT MU-PPDU (receive)
- Spectral intelligence
  - Spectrum monitoring
  - DFS assist to reduce false detections
  - Interference identification/classification
- Precise indoor location positioning (802.11mc) and AoA
- Power save features

3.1.5 WLAN Dual-Radios

- Dual, independent direct-conversion WLAN radios (with dual-MACs and dual-Basebands) support true,simultaneous WLAN network operation at 2 different frequency bands

- Integrated PA
- High dynamic range Rx AGC with support for external LNA
- Optimized Tx gain distribution for linearity and noise performance

3.2 Bluetooth

3.2.1 Bluetooth 2.4 GHz Tx/Rx

- Bluetooth 5.1
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth
- PCM interface for voice applications
- Baseband/radio BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (/4-DQPSK), 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard SDIO and UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (hold, sniff modes, and sniff sub-rating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (2 WBS links)
- Encryption (AES) support

3.2.2 Bluetooth Low Energy (LE)

- Broadcaster, Observer, Central, Peripheral roles
- Supports link layer topology to be master and slave (connects up to 16 links)
- WLAN/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- LE Privacy 1.2
- LE Secure Connection
- LE Data Length Extension
- LE Advertising Extension
- LE Long Range
- 2 Mbps LE
- Direction Finding—Connectionless Angle of Departure (AoD)
- Direction Finding—Connection-oriented Angle of Arrival (AoA)

3.3 Interfaces

- Connecting WLAN and Bluetooth:
  - SDIO 3.0 device interface (4-bit SDIO and 1-bit SDIO) transfer modes at full clock range up to 208MHz)
  - PCIe v3.0 (Gen 3, 2.5/5 Gbps) interface

  Connecting Bluetooth
- High-Speed UART interface
- Peripheral Interfaces
  - 2-Wire serial interface
  - 1-Wire serial interface
- SPI EEPROM interface
  - GPIO interface
- I2S/PCM Interface

4. Applications

- Navigation
- Infotainment
- Telematics
- Hands-free audio
- User interface mirroring
- Remote diagnostics
- Social networking thru car-2-car communication

5. General Specification

5.1 General Specification

Feature	**Description**
Model Name	GOC-N78690P
Bluetooth	
Bluetooth Standard	Bluetooth V5.1
Frequency Band	2402MHz~2480MHz
Interface	UART/PCM/I2S
Antenna Reference	50ohm
Modulation	GFSK, π/4-DQPSK,8DPSK
WIFI	
Standard	IEEE 802.11a/b/g/n/ac/ax
Frequency	2.4 GHz/ 5 GHz
Interface	PCIE
Size	21.00*21.00*2.40mm(L*W*H)
Operating Temperature	-40℃~+85℃
Storage Temperature	-55℃~+125℃
VIO_DUT	1.80V or 3.30V
1V8_DUT	1.80V
3V3_DUT	3.30V
VIO_SD	1.80V or 3.30V

Table 1: General Specification

5.2 WLAN Radio Characteristics

5.2.1 Receive Mode

Table 2: LNA and Rx RF Mixer—2.4 GHz

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	2.4 GHz	2400	--	2500	MHz
Rx input IP3 at RF high gain (In-Band)	Rx input IP3 when LNA in high gain mode at chip input	--	-20	--	dBm
Maximum Rx input level	Maximum Rx input level without device damage	--	--	2	dBm

Table 3: LNA and Rx RF Mixer—5 GHz

Parameter	Condition	Min	Typ	Max	Units
RF frequency range[1]	5 GHz	4900	--	5925	MHz
Rx input IP3 at RF high gain (In-Band)	Rx Input IP3 when LNA in high gain mode at chip input	--	-20	--	dBm
Maximum Rx input level	Maximum Rx input level without device damage	--	--	2	dBm

5.2.2 Transmit Mode

Table 4: Tx Mode—2.4 GHz

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	2.4 GHz	2400	--	2500	MHz
Tx output saturation	Saturation power at chip output	--	26	--	dBm
Tx carrier suppression (CW)	Carrier suppression at chip output	--	-36	--	dB
Tx I/Q suppression with IQ calibration	I/Q suppression at chip output	--	-45	--	dBc

Table 5: Tx Mode—5 GHz

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	5 GHz	4900	--	5925	MHz
Tx output saturation	Saturation power at chip output	--	27	--	dBm
Tx carrier suppression (CW)	Carrier suppression at chip output	--	-36	--	dB
Tx I/Q suppression with IQ calibration	I/Q suppression at chip output	--	-45	--	dBc

5.3 Bluetooth Radio Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Receiver Section					
RF frequency range	--	2.4	--	2.5	GHz
IF frequency	--	--	2	--	MHz

Input IP3 (@ maximum gain of 72 dB)	--	--	-19	--	dBm
Out-of-band blocking	30–2000 MHz	--	-12.5	--	dBm
	2–2.399 GHz	--	-12.4	--	dBm
	2.484–3 GHz	--	-18	--	dBm
	3–12.75 GHz	--	-2.6	--	dBm
RSSI Range	Resolution = 1 dB	--	-90	0	dBm
Input impedance software for ANT -IN	50 Return Loss	--	--	-10	dB
Transmitter Section					
RF frequency range	--	2.4	--	2.5	GHz
Output power @pin	Class 1 without external PA—BDR	--	+13	--	dBm
	Class 1 without external PA—EDR	--	+10	--	dBm
Gain range	Class 1 without external PA	--	30	--	dB
Gain resolution	--	--	0.5	--	dB
Spurious emission (BDR) (in-band)	±500 kHz	--	-20	--	dBc
	±2 MHz	--	-33	--	dBm
	±3 MHz	--	-45	--	dBm
Spurious emission (EDR) (in-band)	±1 MHz	--	-26	--	dBc
	±1.5 MHz	--	-29	--	dBm
	±2.5 MHz	--	-40	--	dBm
Spurious emission (out-of-band)	30–88 MHz	--	-65	-41.25	dBm
	88–960 MHz	--	-65	-41.25	
	0.96–20 GHz All frequencies in this range < -41.25 dBm, except at 2x Bluetooth channel frequency. Measured at pin without external filter.	--	-35	-25	
	Restricted—2.38–2.39 GHz	--	-55	-41.25	
	Restricted—2.4835–2.6 GHz	--	-50	-41.25	
Out-of-band/ Cellular band noise	GSM850 (869–894 MHz)	--	-140	--	dBm/Hz
	GSM900 (925–960 MHz)	--	-140	--	
	GSM DCS (1805–1880 MHz)	--	-135	--	
	GSM PCS (1930–1990 MHz)	--	-135	--	

	GPS (1575.42 ±1.023 MHz)	--	-140	--	
	WCDMA Band I (2110–2170 MHz)	--	-130	--	
	WCDMA Band V (869–894 MHz)	--	-140	--	

Table 6: Bluetooth Radio Specification

6. Pin Diagram And Description

6.1 Pin Diagram

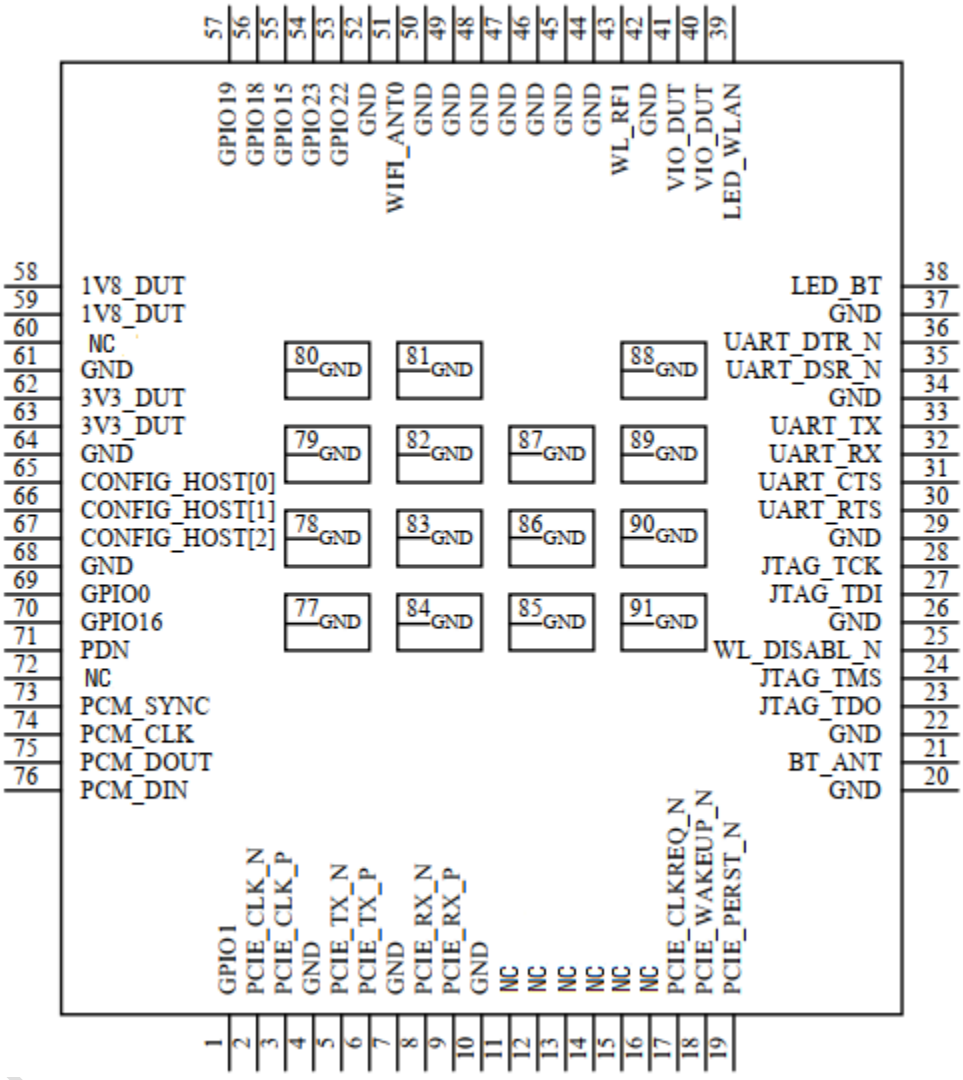

Figure 2: Pin Diagram

6.2 Pin Definition

Pin	Pin Name	Type	Description
1	GPIO1	Input/Output	Programmable input/output line
2	PCIE_CLK_N	Input	PCI Express Differential Clock Input—Negative
3	PCIE_CLK_P	Input	PCI Express Differential Clock Input—Positive

4	GND	GND	Ground
5	PCIE_TX_N	Output	PCI Express Transmit Data—Negative
6	PCIE_TX_P	Output	PCI Express Transmit Data—Positive
7	GND	GND	Ground
8	PCIE_RX_N	Input	PCI Express Receive Data—Negative
9	PCIE_RX_P	Input	PCI Express Receive Data—Positive
10	GND	GND	Ground
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	PCIE_CLKREQ_N	Input/Output	PCIe clock request
18	PCIE_WAKEUP_N	Input/Output	PCIe wake signal(active low)
19	PCIE_PERST_N	Input	PCIe host indication to reset the device (active
20	GND	GND	Ground
21	BT_ANT	RF	BT Antenna
22	GND	GND	Ground
23	JTAG_TDO	Output	JTAG test data
24	JTAG_TMS	Input	JTAG controller select
25	WL_DISABLE_N	Input	Host indication to disable the WLAN function of the device(active low).
26	GND	GND	Ground
27	JTAG_TDI	Input	JTAG test data
28	JTAG_TCK	Input	JTAG test clock
29	GND	GND	Ground
30	UART_RTS	Output	UART_RTS
31	UART_CTS	Input	UART_CTS
32	UART_RX	Input	UART_RXD
33	UART_TX	Output	UART_TXD
34	GND	GND	Ground
35	UART_DSR_N	Input	UART_DSR_N(active low)
36	UART_DTR_N	Output	UART_DTR_N(active low)
37	GND	GND	Ground
38	LED_BT	Output	LED_BT
39	LED_WLAN	Output	LED_WLAN
40	VIO_DUT	Power	1.80V or 3.30V Supply voltage

41	VIO_DUT	Power	1.80V or 3.30V Supply voltage
42	GND	GND	Ground
43	WIFI_RF1	RF	WIFI(2.4G/5G) Antenna
44	GND	GND	Ground
45	GND	GND	Ground
46	GND	GND	Ground
47	GND	GND	Ground
48	GND	GND	Ground
49	GND	GND	Ground
50	GND	GND	Ground
51	WIFI_ANT0	RF	WIFI(2.4G/5G) Antenna
52	GND	GND	Ground
53	GPIO22	Input/Output	Programmable input/output line
54	GPIO23	Input/Output	Programmable input/output line
55	GPIO15	Input/Output	Programmable input/output line
56	GPIO_18	Input/Output	Programmable input/output line
57	GPIO_19	Input/Output	Programmable input/output line
58	1V8_DUT	Power	1.80V Supply voltage
59	1V8_DUT	Power	1.80V Supply voltage
60	NC	NC	NC
61	GND	GND	Ground
62	3V3_DUT	Power	3.30V Supply voltage
63	3V3_DUT	Power	3.30V Supply voltage
64	GND	GND	Ground
65	CONFIG_HOST[0]	Input	This pin is used as a configuration pin.
66	CONFIG_HOST[1]	Input	This pin is used as a configuration pin.
67	CONFIG_HOST[2]	Input	This pin is used as a configuration pin.
68	GND	GND	Ground
69	GPIO_0	Input/Output	Programmable input/output line
70	GPIO16	Input/Output	Programmable input/output line
71	PDN	Input	Full Power-down(active low)
72	NC	NC	NC
73	PCM_SYNC	Input/Output	Output if master/Input if slave
74	PCM_CLK	Input/Output	Output if master/Input if slave
75	PCM_OUT	Output	PCM_DOUT
76	PCM_IN	Input	PCM_DIN
77	GND	GND	Ground
78	GND	GND	Ground

79	GND	GND	Ground
80	GND	GND	Ground
81	GND	GND	Ground
82	GND	GND	Ground
83	GND	GND	Ground
84	GND	GND	Ground
85	GND	GND	Ground
86	GND	GND	Ground
87	GND	GND	Ground
88	GND	GND	Ground
89	GND	GND	Ground
90	GND	GND	Ground
91	GND	GND	Ground

Table 7: Pin Description

6.3 PCB Layout Footprint

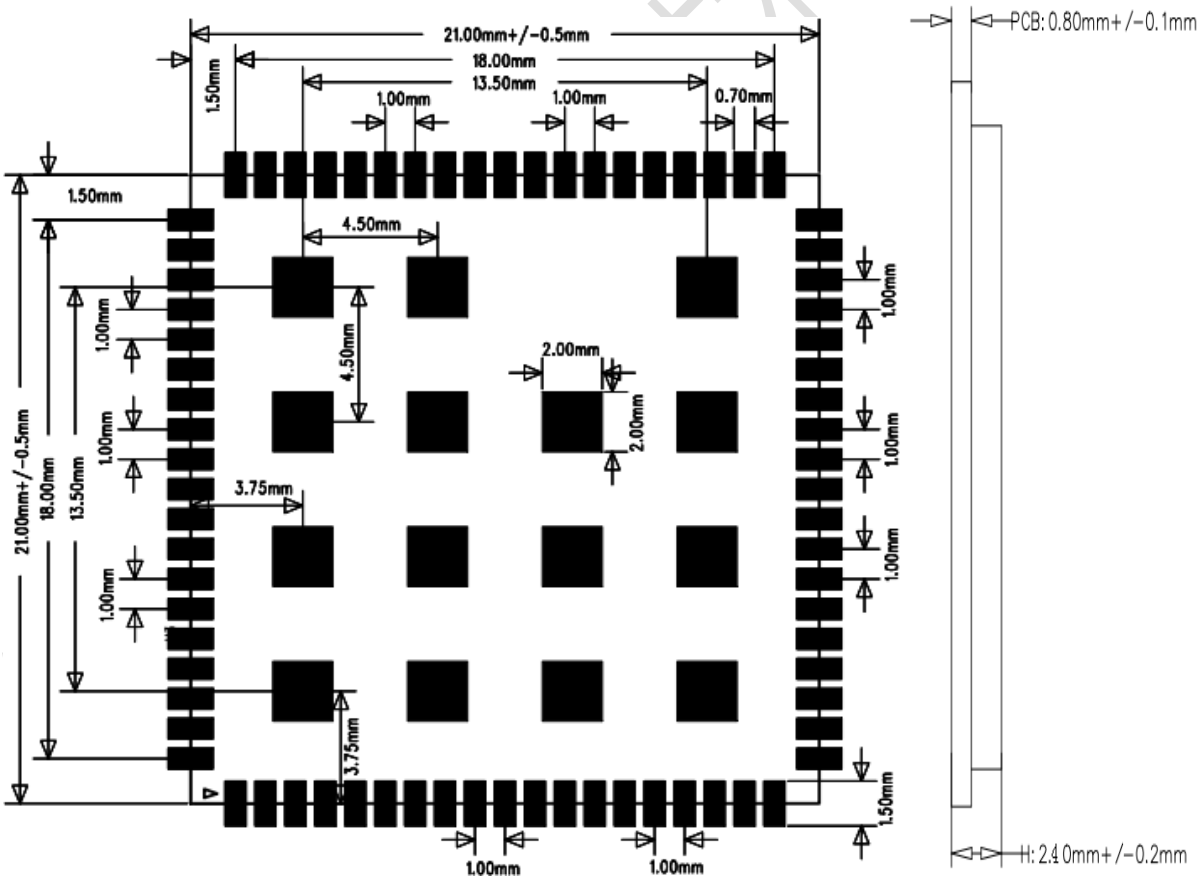

Figure 3: GOC-N78690P PCB Layout Footprint

7. UART Interface

The UART Tx and Rx pins are powered from the VIO voltage supply.

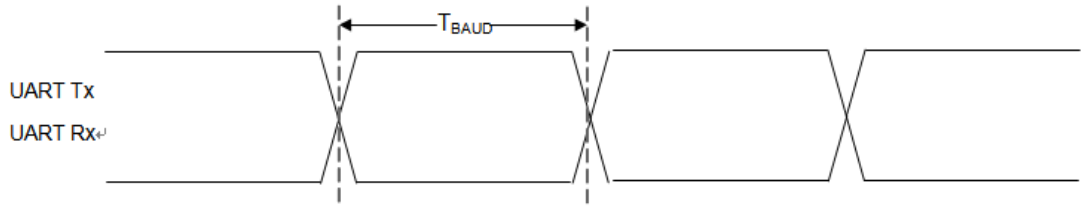

Figure 4: UART Transmit Flow Control Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	40 MHz input clock	250	--	--	ns

Table 8: UART Timing Data[1]

1. The acceptable deviation from the UART Rx target baud rate is ±3%

8. PCM Interface

The PCM pins are powered from the VIO voltage supply.

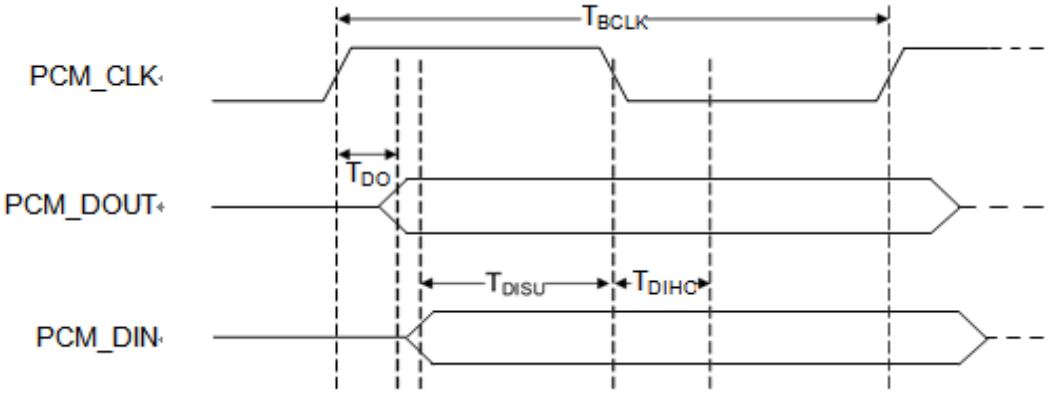

Figure 5: PCM Timing Specification Diagram for Data Signals—Master Mode

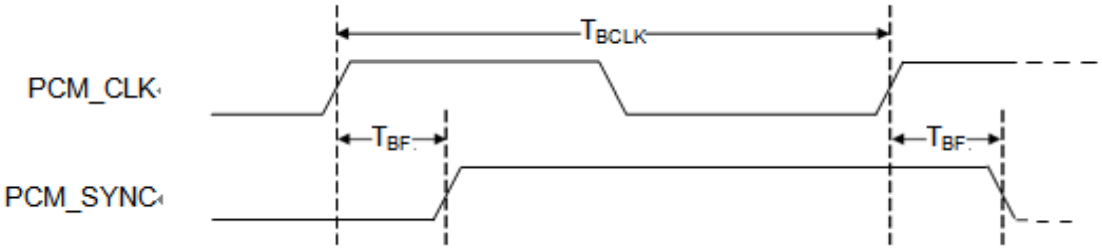

Figure 6: PCM Timing Specification Diagram for Sync Signal—Master Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns

T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

Table 9: PCM Timing Specification Data—Master Mode

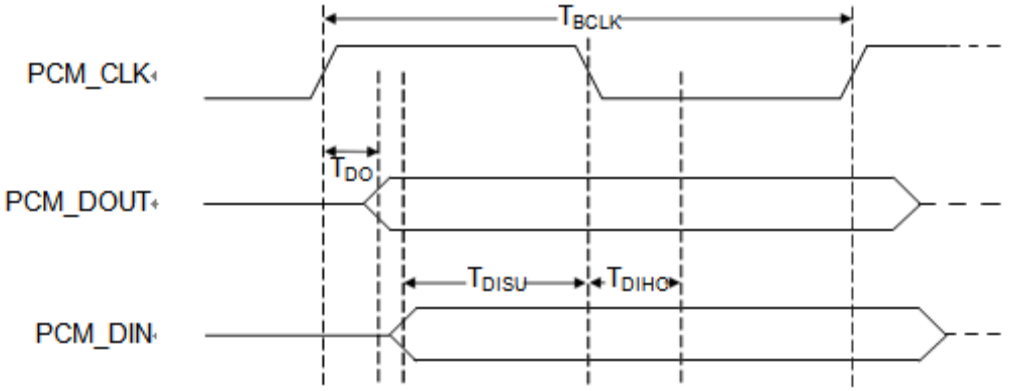

Figure 7: PCM Timing Specification Diagram for Data Signals—Slave Mode

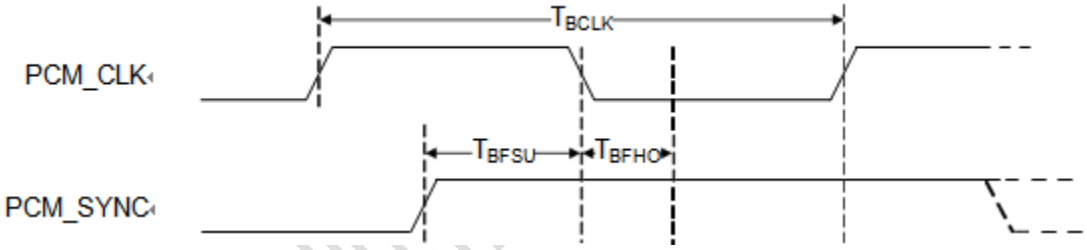

Figure 8: PCM Timing Specification Diagram for Sync Signal—Slave Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

Table 9: PCM Timing Specification Data—Slave Mode

9. Power Sequence

9.1 Power-up Sequence

- When VIO/VIO_RF is 3.3V:
  - VIO/VIO_RF must be good (90%) before or at the same time all other power supplies start ramping up.
  - VIO/VIO_RF must be good (90%) before or at the same time PDn starts ramping up.
- When VIO/VIO_RF is 1.8V, VIO/VIO_RF may ramps up after VPA and at he same time as AVDD18.
- VPA must be good (90%) before or at the same time AVDD18 starts ramping up.
- It is recommended to ramp up AVDD18 100 ms after VPA is good (90%).
- Ramp-up time of VIO/VIO_RF must be <100 ms.
- Ramp-up time of VPA must be <100 ms.
- Ramp-up time of AVDD18 must be <100 ms.
- Ramp-up time of VCORE must be <5 ms.
- All supplies must be monotonic.
- If using an external crystal oscillator, the reference clock must be stable before PDn ramps up.

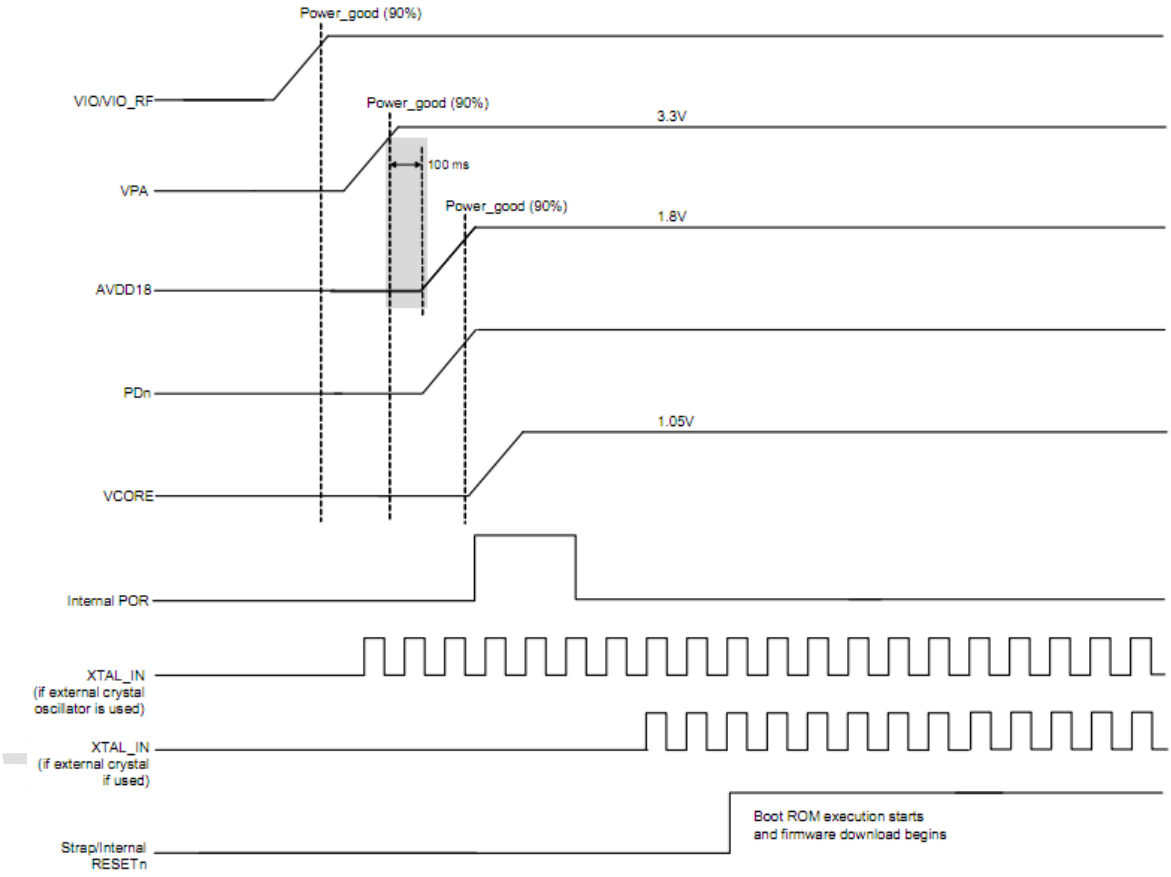

Figure 8: Power-up Sequence

9.2 Power-down Sequence

- To reduce leakage, ramp down AVDD18 before VPA when powering down the SoC.
- One of the following conditions must be met before Power-On Reset (POR) is triggered again:
  - PDn is discharged to less than 0.2V

- VCORE and PDn are discharged to less than 0.2V
- AVDD18 and PDn are discharged to less than 0.2V
- VCORE, AVDD18, and PDn are discharged to less than 0.2V

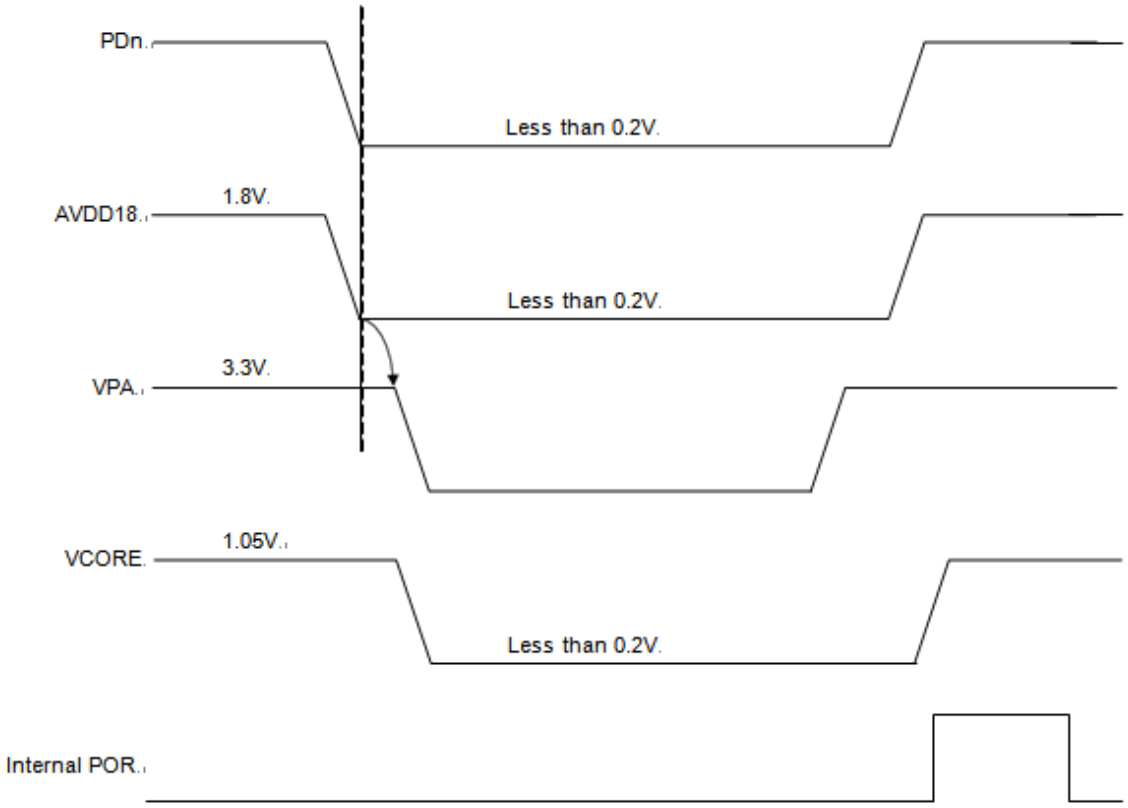

Figure 9: Power- down Sequence

10. PCIE Interface

10.1 Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	399.88	--	400.12	ps
$V_{Tx-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD}+ - V_{TXD}-\|$	0.8	--	1.2	V
$V_{Tx-DIFF-PP-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD}+ - V_{TXD}-\|$	0.4	--	1.2	V
$V_{Tx-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	--	4.0	dB
T_{Tx-EYE}	Tx eye including all jitter sources	0.75	--	--	UI
$T_{Tx-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
$T_{Tx-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.125	--	--	UI

$RL_{Tx-DIFF}$	Tx package plus Si differential return loss	10	--	--	dB
RL_{Tx-CM}	Tx package plus Si common mode return loss	6	--	--	dB
$V_{Tx-CM-AC-P}$	Tx AC common mode voltage	--	20	--	mV
$I_{Tx-SHORT}$	Tx short circuit current limit	--	--	90	mA
$V_{Tx-DC-CM}$	Tx DC common mode voltage	0	--	3.6	V
$V_{Tx-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	--	100	mV
$V_{Tx-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx-RCV-DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$T_{Tx-IDLE-MIN}$	Minimum time spent in electrical idle	20	--	--	ns
$T_{Tx-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	8	ns
$T_{Tx-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle	--	--	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	--	--	1.0	ms
C_{Tx}	AC coupling capacitor	75	--	200	nF

Table 10: PCI Express Tx Output Specifications Data—2.5 GT/s

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	199.94	--	200.06	ps
$V_{Tx-DIFFpp}$	Differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.8	--	1.2	V
$V_{Tx-DIFFpp-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.4	--	1.2	V
$V_{Tx-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	--	4.0	dB
$V_{Tx-DE-RATIO-6dB}$	Tx de-emphasis level ratio (6 dB)	5.5	--	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width Measured relative to rising/falling pulse.	0.9	--	--	UI
T_{Tx-EYE}	Tx eye including all jitter sources	0.75	--	--	UI
$T_{Tx-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz Deterministic jitter only.	--	--	0.15	UI
$T_{Tx-LF-RMS}$	Tx RMS jitter < 1.5 MHz Total energy measured over a 10 kHz–1.5 MHz range.	--	3.0	--	ps RMS
$T_{Tx-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.15	--	--	UI
$RL_{Tx-DIFF}$	Tx package plus Si differential return loss (0.05–1.25 GHz)	10	--	--	dB
	Tx package plus Si differential return loss (1.25–2.5 GHz)	8	--	--	

RL_{Tx-CM}	Tx package plus Si common mode return loss	6	--	--	dB
$V_{Tx-CM-AC-PP}$	Tx AC common mode voltage	--	--	100	mVPP
$I_{Tx-SHORT}$	Tx short circuit current limit	--	--	90	mA
$V_{Tx-DC-CM}$	Tx DC common mode voltage	0	--	3.6	V
$V_{Tx-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	--	100	mV
$V_{Tx-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage $V_{Tx-IDLE-DIFF-DC} = \|V_{Tx-Idle-D+} - V_{Tx-Idle-D-}\| \leq 20$ mV	0	--	20	mV
$V_{Tx-IDLE-DIFF-DC}$	DC electrical idle differential output voltage $V_{Tx-IDLE-DIFF-DC} = \|V_{Tx-Idle-D+} - V_{Tx-Idle-D-}\| \leq 5$ mV	0	--	5	mV
$V_{Tx-RCV-DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$T_{Tx-IDLE-MIN}$	Minimum time spent in electrical idle	20	--	--	ns
$T_{Tx-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	8	ns
$T_{Tx-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid differential signaling after leaving electrical idle	--	--	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	--	--	1.0	ms
C_{Tx}	AC coupling capacitor	75	--	200	nF

Table 11: PCI Express Tx Output Specifications Data—5 GT/s

10.2 Differential Rx Input Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	399.88	--	400.12	ps
$V_{Rx-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture	0.175	--	1.2	V
$V_{Rx-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.175	--	1.2	V
T_{Rx-EYE}	Rx eye time opening Minimum eye time at Rx pins to yield a 10^{-12} BER.	0.40	--	--	UI
$T_{Rx-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between median and deviation from median	--	--	0.3	UI
$V_{Rx-CM-ACp}$	AC peak common mode input voltage	--	--	150	mV
$RL_{Rx-DIFF}$	Differential return loss	15	--	--	dB
RL_{Rx-CM}	Common mode return loss	0	--	3.6	dB
$Z_{Rx-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{Rx-DC}	DC input impedance	40	50	60	W
$Z_{Rx-HIGH-IMP-DC}$	Powered down DC input impedance	200	--	--	k
$V_{Rx-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65	--	175	mV

$T_{Rx-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
$L_{Rx-SKEW}$	Total skew	--	--	20	ns

Table 12: PCI Express Rx Input Specifications Data—2.5 GT/s

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	199.94	--	200.06	ps
$V_{Rx-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture	0.120	--	1.2	V
$V_{Rx-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.100	--	1.2	V
$T_{Rx-TJ-CC}$	Maximum Rx inherent total timing error for common Refclk Rx architecture	--	--	0.40	UI
$T_{Rx-TJ-DC}$	Maximum Rx inherent total timing error for data clocked Rx architecture	--	--	0.34	UI
$T_{Rx-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error for common Refclk Rx architecture	--	--	0.30	UI
$T_{Rx-DJ-DD-DC}$	Maximum Rx inherent deterministic timing error for data clocked Rx architecture	--	--	0.24	UI
$T_{Rx-MIN-PULSE}$	Minimum width pulse at Rx Measured to account for worst Tj at 10^{-12} BER.	0.6	--	--	UI
$V_{Rx-CM-ACp}$	AC peak common mode input voltage	--	--	150	mV
$RL_{Rx-DIFF}$	Differential return loss	15	--	--	dB
RL_{Rx-CM}	Common mode return loss	0	--	3.6	dB
$Z_{Rx-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{Rx-DC}	DC input impedance	40	50	60	W
$Z_{Rx-HIGH-IMP-DC}$	Powered down DC input impedance	200	--	--	k
$V_{Rx-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
$L_{Rx-SKEW}$	Total skew	--	--	20	ns

Table 13: PCI Express Rx Input Specifications Data—5 GT/s

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Ratings	Min	Typical	Max
VIO_DUT	-	1.80V	1.98V
	-	3.30V	3.63V
1V8_DUT	-	1.80V	2.16V
3V3_DUT	-	3.30V	3.96V

Table 14: Absolute Maximum Ratings

11.2 Recommended Operating Conditions

Operating Conditions	Min	Typ	Max
Storage Temperature	-55℃	-	125℃
Operating Temperature	-40℃	-	85℃
VIO_DUT	1.71V	1.80V	1.89V
	3.14V	3.30V	3.46V
1V8_DUT	1.71V	1.80V	1.89V
3V3_DUT	3.14V	3.30V	3.46V

Table 15: Recommended Operating Conditions

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≦260 ℃

Number of Times : 5~10sec

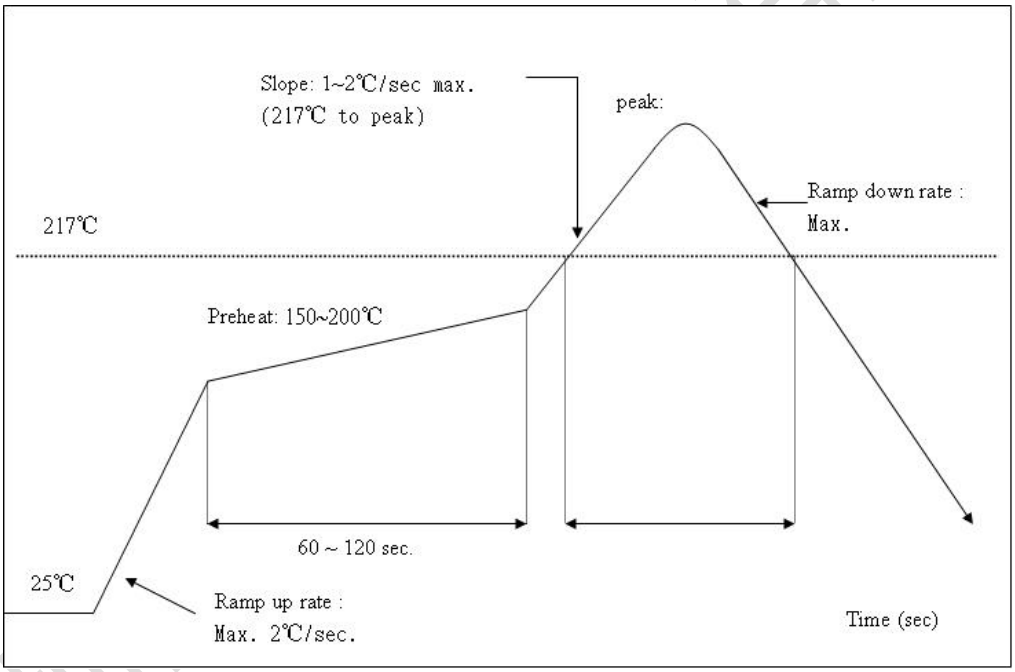

Figure 10: Recommended Reflow Profile

13. PCB Layout Recommendation

13.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

13.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX UART_TX UART_CTS UART_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

13.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

PCM_SYNC PCM_CLK PCM_DOUT PCM_DIN

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

13.4 Power Trace Lines Layout Guideline

- VIO_DUT Trace Width: 30mil
- 1V8_DUT Trace Width: 30mil
- 3V3_DUT Trace Width: 30mil
- VIO_SD Trace Width: 25mil

13.5 Ground Lines Layout Guideline

- A Complete Ground in Ground Layer.
- Add Ground Through Holes to GOC-N78690P Module Ground Pads
- Decoupling Capacitors close to GOC-N78690P Module Power and Ground Pads

14. Module Part Number Description

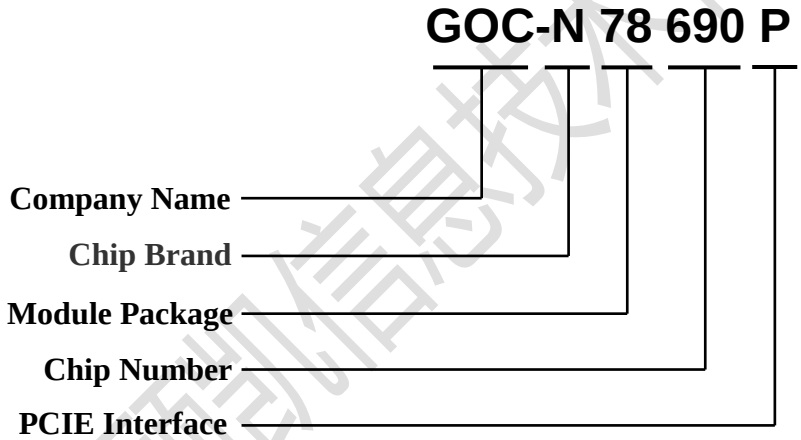

Figure 11: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

15. Ordering Information

Part Number	Description	Remark
GOC-N78690P V1.1	BT+WIFI Module	

Table 16: Ordering Information

16. Packaging Information

16.1 Net Weight

The module net weight: TBD

16.2 Package

TBD

16.3 Storage Requirements

1）Temperature: 22~28℃;
2 ）Humidity: <70%（ RH）;
Vacuum packed and sealed in good condition to ensure 12 months of welding.

16.4 Humidity Sensitive Characteristic

1） MSL: 3 level
2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).
3） Handling, storage, and processing should follow IPC/JEDECJ-STD-022